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Leitprojekt H2Giga

Bundesministerium für Forschung, Technologie und Raumfahrt

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Optimized Semiconductor Power Modules for Electrolyzer System Applications

Varun Raghunath I 26 September 2025

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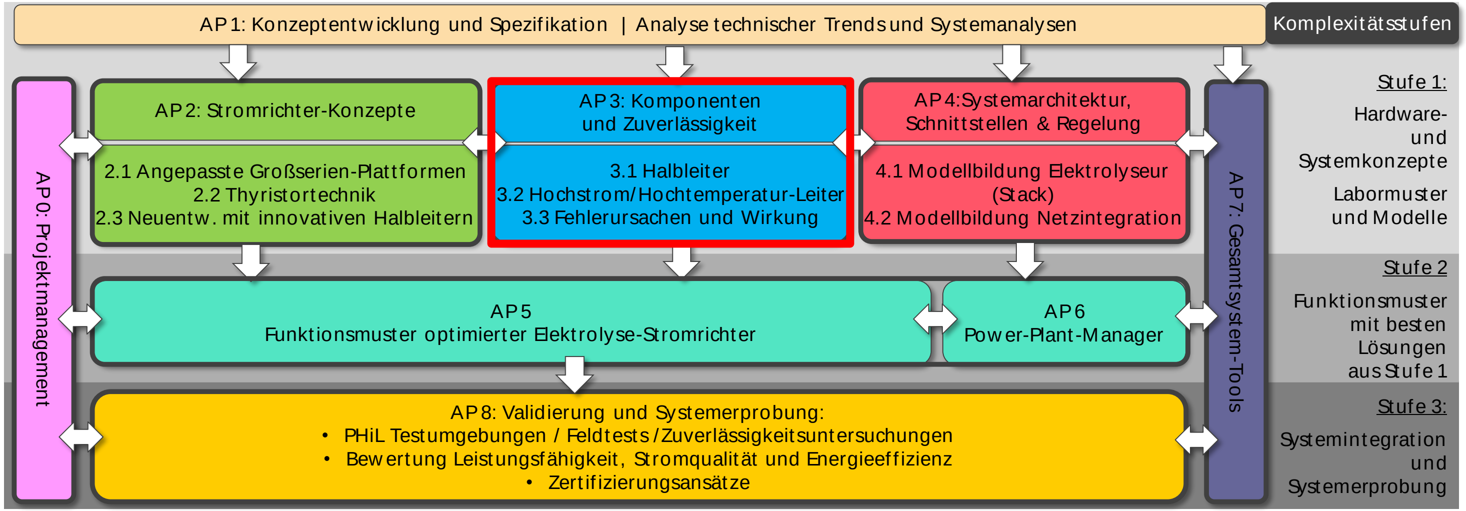
Overview Infineon Work packages



- Collaboration in AP 0, AP 1, AP 2 und AP 8
- Focus on AP 3.1 Semiconductors

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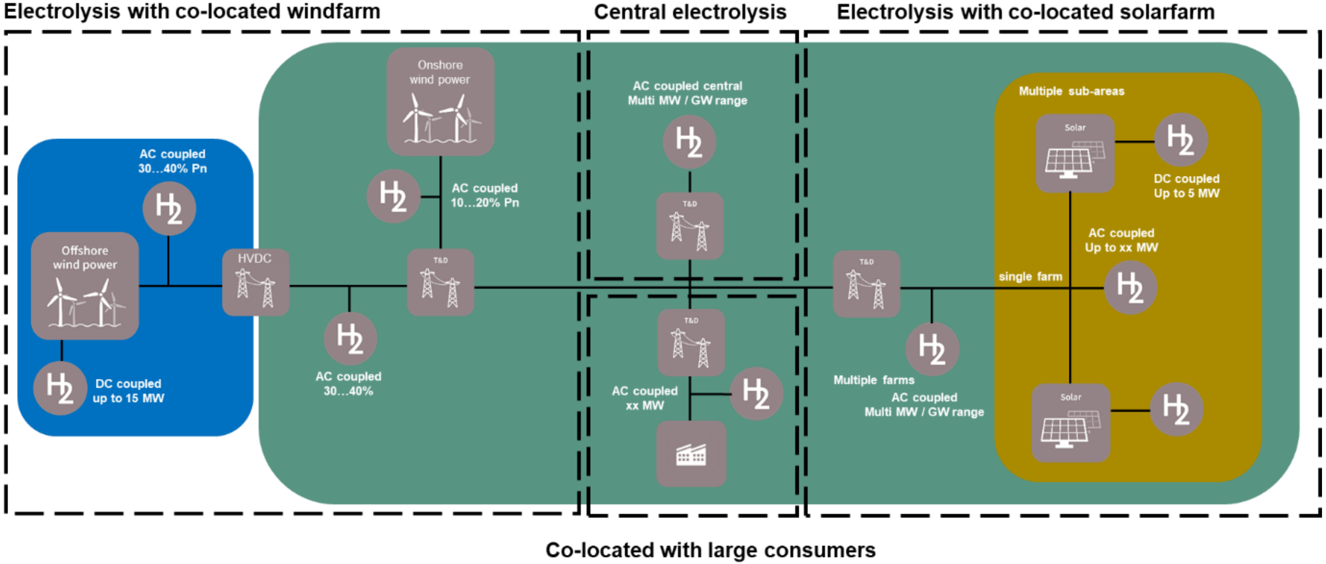
AP 2 Power converter concepts and application landscape from Infineon perspective



- Diverse in terms of
- Location
- Output voltage level/type
- Operating mode

- Source: own illustration

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AP 3.1.1 Semiconductor technologies
Comparison between Si and SiC material parameters

Material Parameter	Si	SiC	Effects for SiC (at same voltage /current)	Required adaptations for SiC module
Bandgap (eV)	1,1	3,3	+ Smaller chips + Better switching losses - Higher electric field at chip edges	Innovative solution for edge termination
Thermal conductivity (W/mK)	150	490	- Higher thermal gradients on the back of the chip	Change from solder to sinter connection technology
Heat dissipation coefficient (ppm/K)	2,3	3,5	- Higher load through thermal expansion	New requirement for interconnect technologies
Youngs Modulus (GPa)	130	450	- Higher load through higher stiffness	New requirement for interconnect technologies

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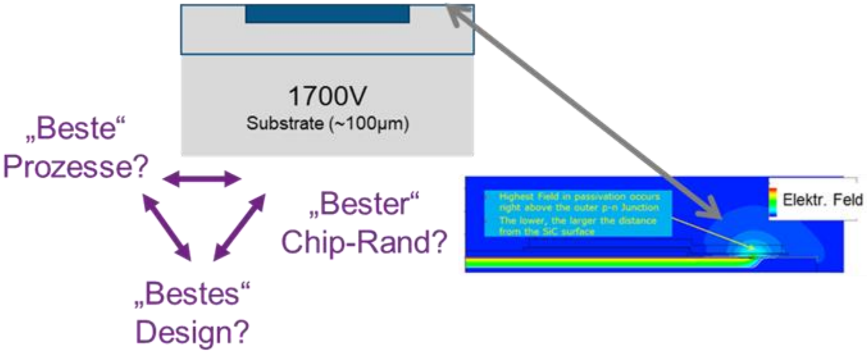
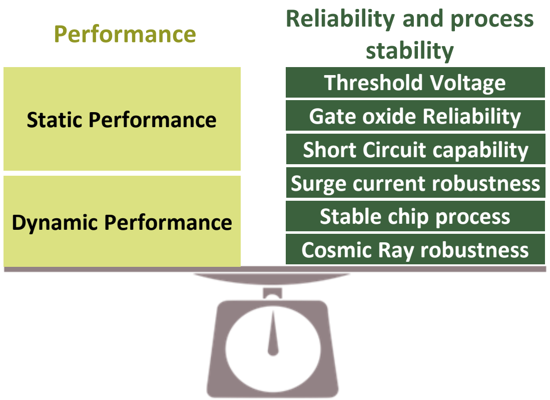
AP 3.1.1: Semiconductor technologies Fundamental considerations





- Adaptation of >100 individual processes to achieve a reliable design point
- Electrical fields at the chip edge are significantly higher than with Si
  - Avoidance of field peaks
  - Examination of the passivation (chip and module)

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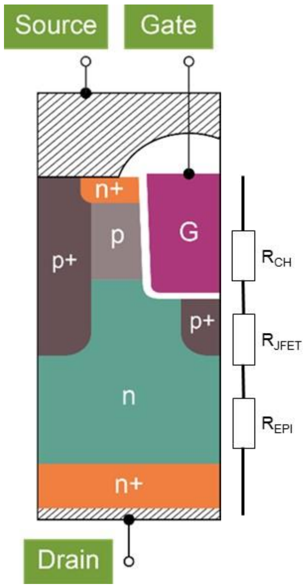
AP 3.1.1: SiC MOSFET – fundamental design trade-offs



- Channel resistance R_{CH} can be optimized through the front end processes
- JFET resistance R_{JFET} can be adjusted by optimizing the doping
- Drift zone resistance R_{EPI} can be adjusted with the thickness of the epitaxial layer and the doping
  - This has direct effect on the blocking voltage
    - Electrical field at the gate oxide
    - Robustness against cosmic radiation

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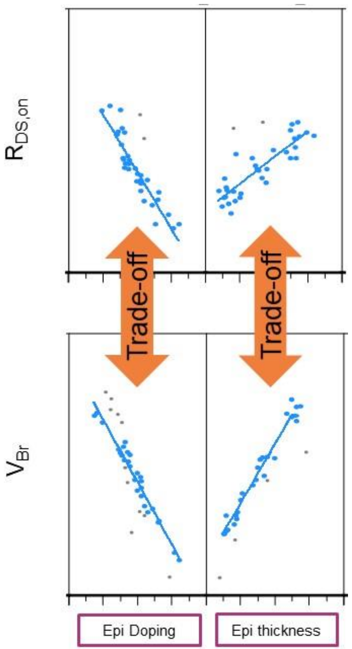
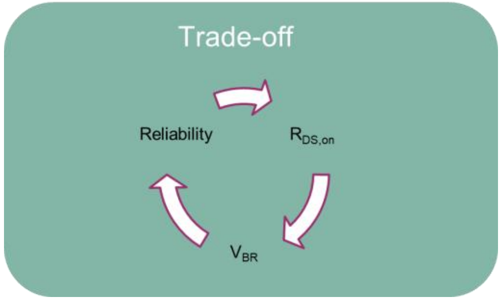
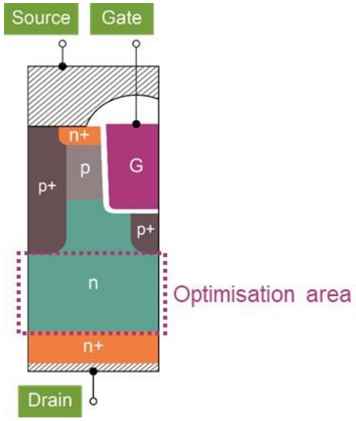
AP 3.1.1: Front end tests – focus on $R_{DS,ON}$ and V_{Br}



- Result for $R_{DS,ON}$
  - Higher dependence on doping of the drift zone
- Result for V_{Br}
  - High dependence on doping and thickness of the drift zone





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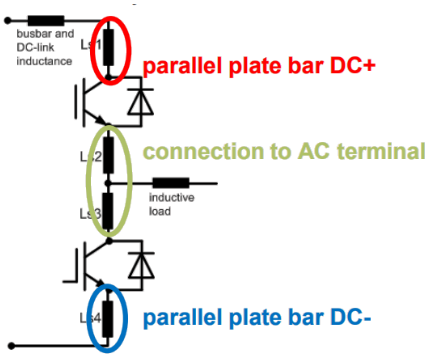
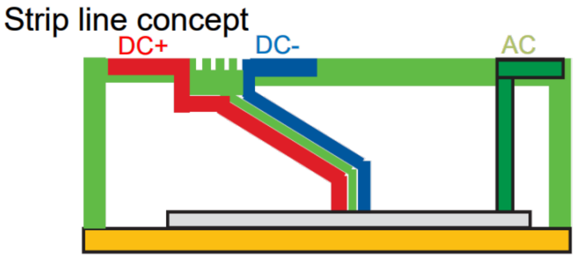
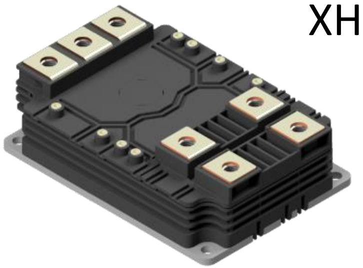
AP 3.1.2: Module for hybrid thyristor topologies

- Intensive discussion with SMA and TUD
  - First indications of voltages >1.5kVDC (up to 2kVDC)
  - Considerations for a high current 2.3kV and 3.3kV SiC MOSFET module





XHP™ 2



<u>HyLeiT AP 3.1.2 Sample modules</u>

$R_{DS,ON}$ = 1mOhm @25°C

I_{NOM} = 2000 A

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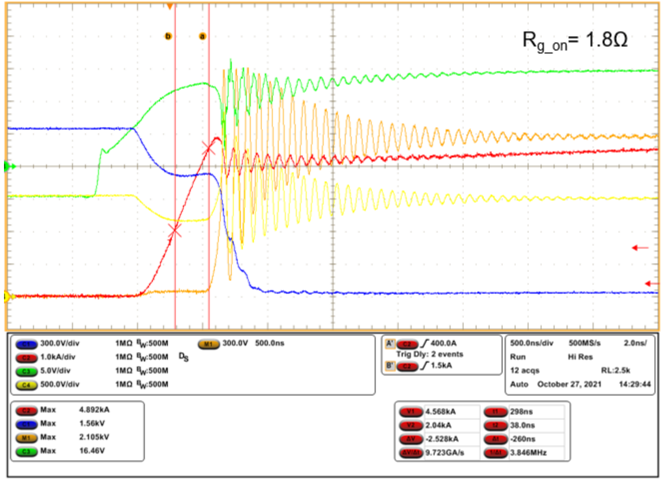
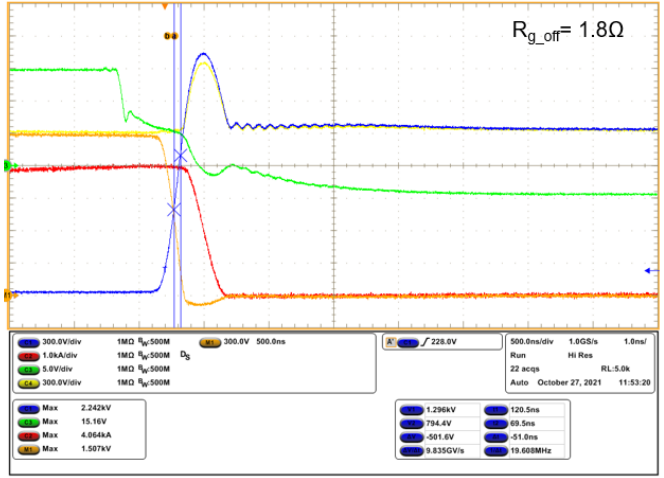
AP 3.1.2: Characterization of module

Switching curves 1.5 kV / 2x I_{nom} / 150°C (early prototypes)

Turn ON



Turn OFF



Low side

Ch1 (Blue): U_{DS}

Ch2 (Red): I_D

Ch3 (Green): U_{GS}

High side

M1 (Orange): $U_{DS,\ Bodydiode}$

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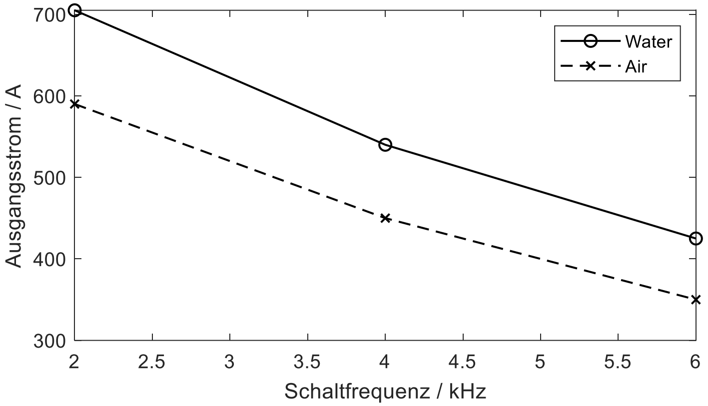
AP 3.1.2: Scaling and simulating in application

Performance estimation HyLeiT-Module

Output current vs switching frequency



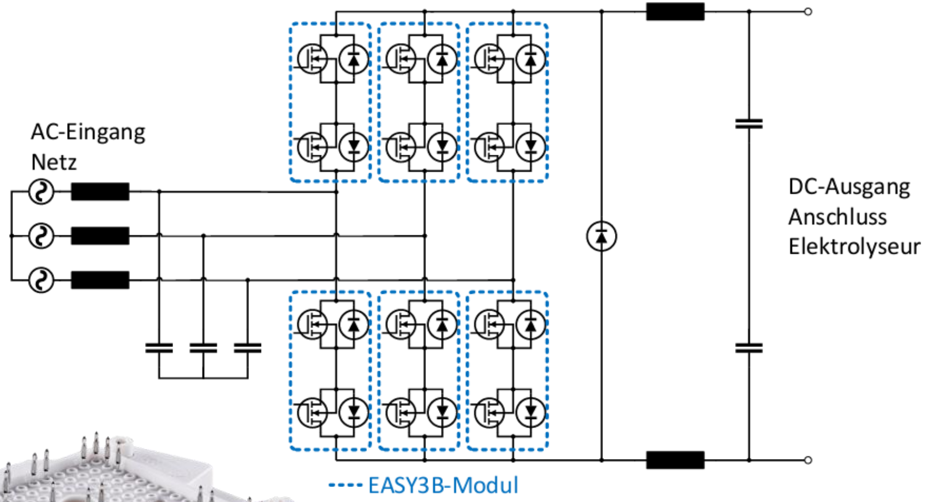
U_{DC} = 1.2 kV
U_{OUT} = 800 V
f_{SW} = 2...6 kHz

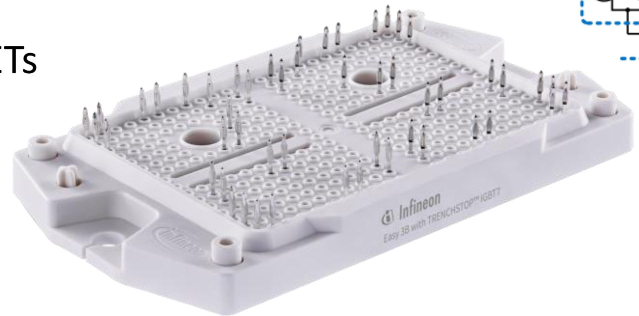
Number of required modules (28 kA)

Liquid cooling:	40 – 65 (17 K/kW)
Forced air cooling:	48 – 80 (50 K/kW)

AP 3.1.3: Module for innovative rectifier

- Topology decision from H-RBS / IEE
  - Six switch buck converter
- 1200V SiC MOSFET
- Easy 3B package
  - Common source MOSFETs





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Thank you

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